A Charge-Pump-based Digital LDO Employing an AC-Coupled High-Z Feedback Loop Towards a sub-4fs FoM and a 105,000x Stable Dynamic Current Range

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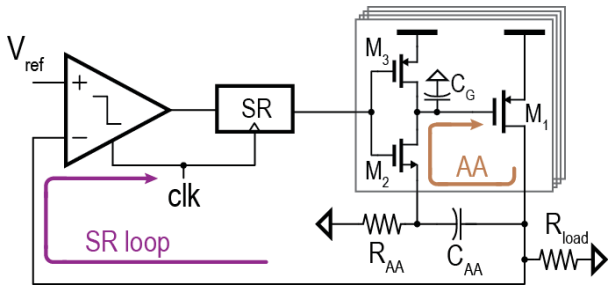
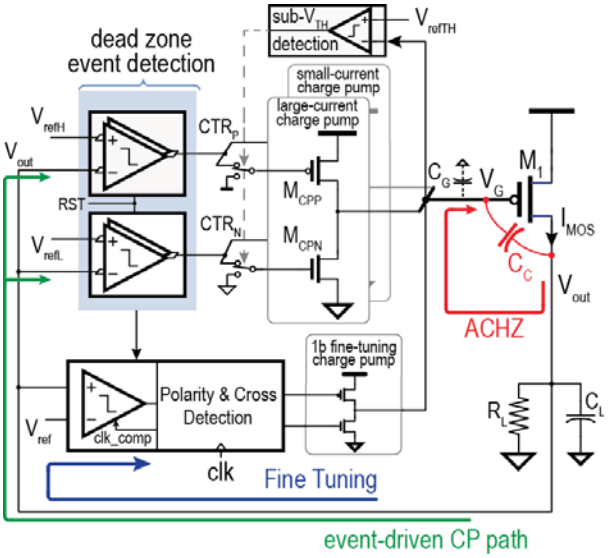
***Abstract*—This paper presents an event-driven charge-pump-based digital LDO (DLDO) with an AC-coupled high-Z (ACHZ) feedback loop. The proposed DLDO responses in less than a clock cycle during load transients, achieving response and settling times of 6.9ns and 65ns, respectively, all at a 4.9μA quiescent current for a sub-4fs FoM. Thanks to the fine-tuning, sub-Vt detecting, overflow current suppressing, and g_m-adjusting weighted-charge-pump-based design, the ripple is measured to be <15mV, and a 105,000x stable load range (1μA to 105mA) is obtained in a 65nm prototype.**

I. Introduction

Digital low-drop out regulators (DLDOs) have been recently shown to operate at lower supply voltages than analog LDOs, while also offering better scalability, process portability, and superior resilience to process variation [1-4]. However, conventional shift-register-based N-bit DLDOs require at least N clock cycles to respond to sudden full-scale load changes [1], which may be too slow for the increasingly stringent demands of modern digital loads. Unfortunately, increasing the clock speed in register-based designs leads to high quiescent power and, without careful compensation, can result in stability issues. Event-driven control via continuous-time comparators can help DLDOs respond more quickly [2], yet require energy-expensive multi-bit quantizers and have non-negligible delay through complicated control logic. An analog-assist (AA) loop, can be employed to achieve a sub-clock-cycle response [3], as depicted in Fig. 1(a). However, in this case a large capacitor and resistor are required, and, unfortunately, the loop compensation current degrades as the number of power PMOS transistors are disabled at low output currents. A NAND-gate-based analog path (NAP) with NMOS output [4] can provide enhanced compensation at low output currents, but the output current range and input/output voltage range is limited to 41x and 150mV in [4], respectively.



(a)



(b)

Fig. 1: (a) Conventional DLDO with analog-assist (AA) loop. (b) Proposed charge-pump-based DLDO with ACHZ loop.

To achieve a sub-clock-cycle response time, yet also minimize area while efficiently operating over a wide current range, this paper presents a DLDO, shown in Fig. 1(b), that employs: 1) an event-driven charge-pump (CP) path with time-interleaved continuous-time comparators that decouple the clock-speed/response-time trade-off and thus obviates the need for fast clocks, multi-bit quantizers, and energy- and area-expensive shift registers towards a <4fs FoM; 2) a AC-coupled high-Z (ACHZ) feedback loop that bypasses the power PMOS transistor to facilitate 3.7x higher compensation current than an AA loop; 3) an overflow current suppression technique via the ACHZ loop that helps decrease settling time by 56% to 65ns and provide stability; and 4) a low-current detection loop that provides sub-Vt conduction compensation and achieves stable operation over a 105,000x load current range; 5) utilizing the g_m-I_D relationship of the power PMOS transistor driven by the charge-pump to compensate the increased load impedance and suppress the ripple amplitude at low I_{load}, achieving a <15mV ripple amplitude over the entire load range.

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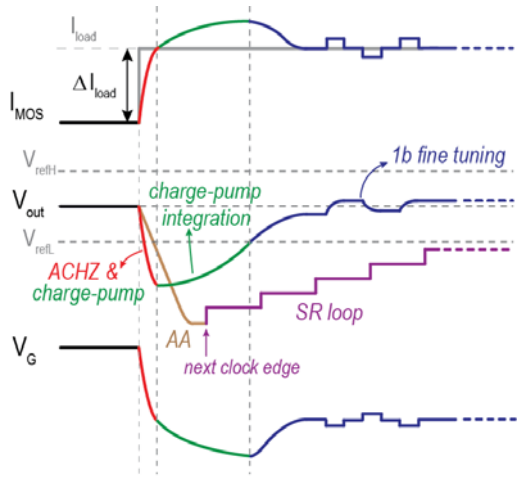
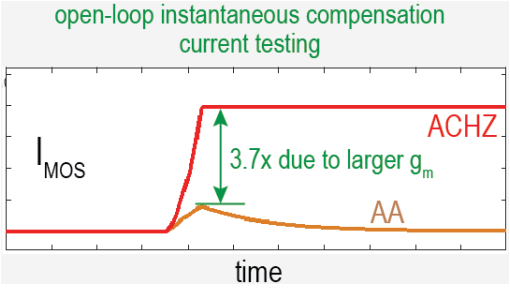
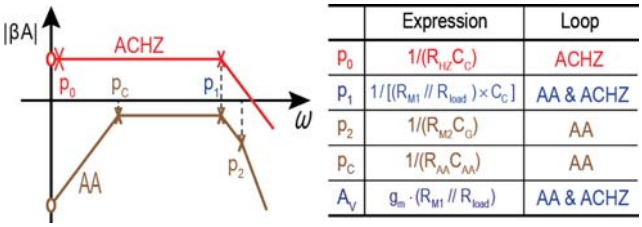


(a)



(b)

Fig. 2: (a) Transient response of the proposed DLDO (b) open-loop instantaneous compensation current testing of ACHZ and AA loop.



	Expression	Loop
P_0	$1/(R_{HZ}C_C)$	ACHZ
P_1	$1/[(R_{M1} // R_{load}) \times C_C]$	AA & ACHZ
P_2	$1/(R_{M2}C_G)$	AA
P_C	$1/(R_{AA}C_{AA})$	AA
A_V	$g_m \cdot (R_{M1} // R_{load})$	AA & ACHZ

Fig. 3: Bode plot of ACHZ and AA loop.

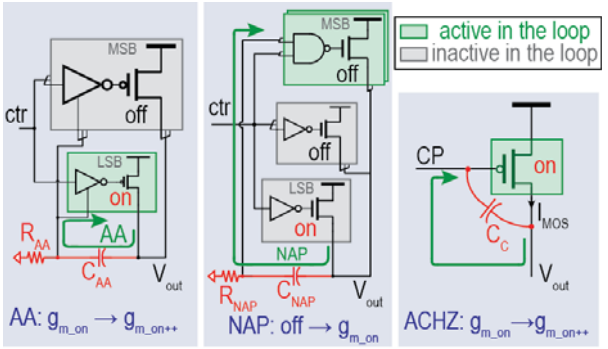


Fig. 4: AA, NAP and ACHZ loop compensation comparison.

II. SYSTEM DESIGN AND ANALYSIS

A. Architecture and Working Flow

The architecture of the proposed DLDO is shown in Fig. 1(b). In contrast to conventional DLDOs that utilize arrays of PMOS power transistors (Fig. 1(a)), the proposed design utilizes a single PMOS power transistor, M_1, driven by a pair of CPs, which in turn are driven by a pair of time-interleaved dynamic-inverter-based continuous-time comparators setting upper and lower regulations bounds (V_{refH} and V_{refL}) of the deadzone. A capacitor C_C is set across the power transistor M_1 to form the ACHZ loop. A clocked comparator compares the output voltage with V_{ref}, and the result is used to control the fine-tuning CP for 1b regulation per cycle.

During steady state, when V_{out} is within the deadzone between bounds, the CPs are disabled, and their output, V_G, is high-impedance, with charge stored on C_C and parasitic capacitance C_G. The ACHZ loop is formed by directly AC coupling V_{out} to V_G via C_C. During a load transient, any droop experienced at V_{out} will, thanks to the high-Z CP output, directly couple to V_G with efficiency set by $C_C/(C_C+C_G)$, thereby lowering the gate of M_1 to provide near-instantaneous compensation current, as shown in Fig. 2(a). The high V_{out}-to-V_G coupling efficiency and charge-pump architecture provide two important benefits: 1) only a small C_C of 40pF is required to achieve over 90% coupling efficiency, even for a 105mA-capable PMOS; and 2) a larger compensation current can be provided and maintained over long time scales, as shown in the open loop simulations in Fig. 2(b). When V_{out} falls below V_{refL}, the comparator is triggered, which turns on M_{CPN} for continuous time integration, further discharging V_G. After V_{out} settles to V_{refL}, the main CPs are shut down, and a clocked comparator compares V_{out} with V_{ref} to control an auxiliary 1b fine-tuning CP to regulate V_{out} by 1 LSB per cycle, which is turned off after V_{out} settles to V_{ref} to avoid limit-cycling.

B. Speed, Dynamic Range and Ripple Improvement

As noted in [3], an AA loop has three poles (Fig. 3), and thus the loop gain, A_V=g_m*R_{out}, is set <1 for stability reasons. The proposed ACHZ loop has only two poles, and the pole at V_G (p_0), which is close to origin due to the high-Z node, is cancelled by the zero introduced by C_C. Thus, the ACHZ loop is inherently stable. This means the loop gain can be set to >1 to obtain a larger g_m, improving compensation current by 3.7x over an AA loop for $I_{load,initial}$=5mA, as shown in Fig. 2(b). Unfortunately, when the load current is small, only a few active transistors in the AA loop can provide compensation current during load transient. While MSB transistors in the NAP loop are involved during the load transient, the MSB transistors need to be turned from off to on, which degrade the compensation strength, as shown in Fig. 4. In the proposed design, the voltage droop is coupled to the sole power transistor, thus providing full compensation capabilities at all current levels.

For conventional shift-register DLDOs, a faster clock allows a faster response speed. However, when f_{clk} is much larger than f_L, the shift register would accumulate more zeros or ones than necessary, which can result in an oscillatory response or

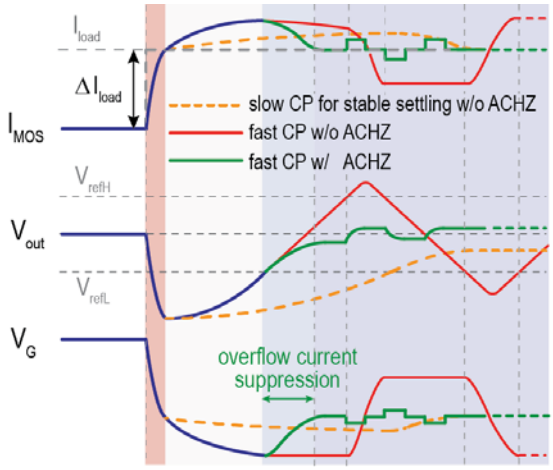


Fig. 5: Load transient waveforms comparison w/ and w/o ACHZ loop.

even make the system unstable. In the proposed design, this stability problem could occur if the charging or discharging speed in the charge pump is too fast. As shown in Fig. 5, after the current provided by the power PMOS (I_{MOS}) equals I_{load}, I_{MOS} continues increasing and V_{out} starts to settle back. Without C_C, V_{out} will settle and reach a steady state with the help of the dead zone. Increase the CP discharging speed will reduce the settling time, but at the risk that V_{out} will pass the deadzone and oscillate between the two boundaries. Fortunately, including the ACHZ loop can help increase the CP current without compromising stability. For example, when V_{out} enters the dead zone, the CP is shut off, and the ACHZ loop is activated, which recouples V_{out} to V_G to suppress the overflow current and help the settling. As a result, much faster CPs can be employed than without ACHZ, reducing settling time by 56%. Note, however, that the g_m of M_1 becomes very small when it enters the sub-Vt region, and thus the overflow current suppression loop is less effective. To combat this, a sub-Vt detection circuit disables the large-current CP, extending the stable operation range down to 1μA, for an effective 6.6b resolution improvement.

When operating in the continuous-time 1b fine-tuning mode, small ripple can be achieved over the entire output range. Since the low g_m at low I_{load} results in less ΔI_{MOS} in each clock cycle during continuous-time 1b fine-tuning mode, the increased load resistance is naturally compensated. Thus, unlike array-based DLDOs, the ripple amplitude of the proposed DLDO is small over the entire output range. During the continuous-time 1b fine-tuning mode, due to the small-size transistors in the fine-tuning CP, the impedance at node G is larger than 4MΩ, together with the low-latency event-driven CP path, the load transient voltage droop difference is less than 3mV compared to the non-continuous mode.

III. Comparator Implementation and Timing

A time-interleaved dynamic-inverter-based comparator is designed based on [2] to perform the continuous-time detection. The inverter-based comparator has the advantages of low

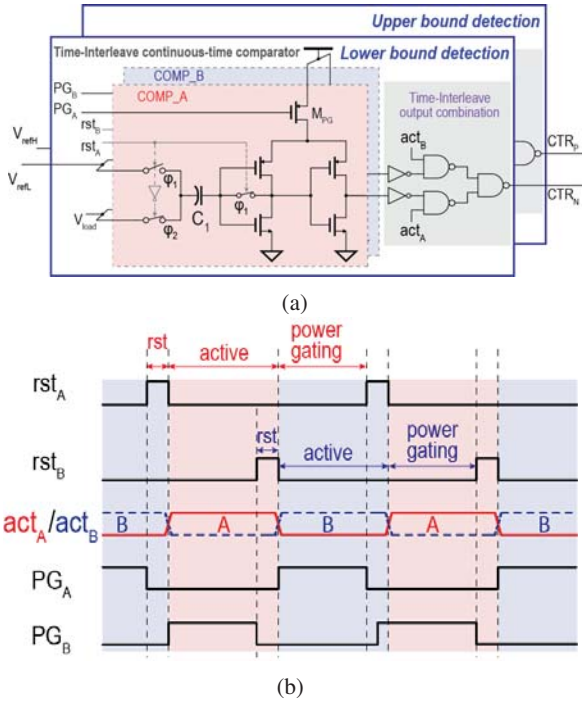


Fig. 6: Schematic(a) and timing diagram(b) of the event-driven charge pump path.

offset, low power, and no need for a current source. However, it has to be reset during operation to refresh the charge stored on the sampling capacitor, which interrupts the detection and may produce an error code [2]. By time-interleaving two of these comparators, a continuous-time operation is enabled throughout the reset phase (Fig. 6(a)). As shown in Fig. 6(b), when COMP_A is active, COMP_B is powered down by M_{PG} to save power, yet is reset prior to the next activation to refresh the charge on sampling capacitor, C_1. Then at the beginning of the next phase, COMP_B is activated and COMP_A is powered down to save power.

IV. Measurement Results

The proposed DLDO is fabricated in 65nm with a total capacitance of 42pF (40pF for C_C and 2pF for the comparators). The DLDO consumes a quiescent current of 4.9μA. The measured transient response for ΔI_{load}=100mA with a 10ns edge rate (i.e., 10mA/ns, which is the fastest edge rate amongst previously reported low-FoM and high-current DLDOs as shown in Table I) is shown in Fig. 7, demonstrating 6.9ns and 65ns response and settling times, respectively, with V_{droop}=88mV for a FoM of 1.8fs. Thanks to the ACHZ and fast CP loops, the DLDO can respond even before the end of the current transient, rendering in this case a response time that is faster than the edge rate. To characterize the worst-case FoM and push the DLDO at edge rates beyond what have been reported in the literature, especially for high-current DLDOs, a ΔI_{load}=100mA was also tested for a 1ns edge. It should be noted that in this case, large *input* droop is also observed in simulations due to finite bondwire inductance and power network resistance (Fig. 8), which has nothing to do with the DLDO design itself, but does serve to reduce the measured

Table. I. Comparison with current state-of-the-art DLDOs

Design	Salem ISSCC'17	Huang ISSCC'17	Ma ISSCC'18	Tsou ISSCC'17	Kundu ISSCC'18	This Work			
Active area [mm^2]	0.102	0.03	0.006	0.19	0.03	0.04			
Process [nm]	65	65	28	40	65	65			
Architecture	BS+PD	AA+SR	NAP+SR	TB+TE	VCO based	Event-Driven charge pump+DCHZ			
V_{in} [V]	0.5-1	0.5-1	0.4-0.55	0.6-1.1	0.6-1.2	0.5-1			
V_{out} [V]	0.3-0.45	0.45-0.95	0.35-0.5	0.5-1	0.4-1.1	0.45-0.95			
Load range	100nA-2mA (20,000x)	0.2mA-13mA (65x)	0.5mA-20.5mA (41x)	1mA-201mA (201x)	20mA-100mA (5x)	1μA-105mA (105,000x)			
Load range with η>90%	33.6μA-2mA (60x)	N.R.	N.R.	N.R.	28mA-100mA (3.5x)	50μA - 105mA (2100x)			
C_L/total C [nF]	0.4/0.4	0/0.1	0/0.024	20/20	0.04/0.04	0/0.042			
Quiescent current [μA]	14	3.2	0.81	98.5	800	4.9			
Clock frequency	200MHz	10MHz	1MHz	N.R.	3.9MHz	1MHz			
Load transient current/ load step edge time	Load current range <50mA			Load current range (>50mA)					
	1.06mA/1ns* (1.06mA/ns)	10mA/1ns* (10mA/ns)	20mA/3ns* (6.6mA/ns)	200mA/1000ns (0.2mA/ns)	50mA/800ns (0.0625mA/ns)	100mA/1ns (100mA/ns)	100mA/10ns (10mA/ns)	100mA/30ns (3.33mA/ns)	100mA/60ns (1.67mA/ns)
V_{droop} [mV] for load transient test	40	105	117	36	148	185	88	56	36
FOM† [fs]	199,000	230	5.7	1,780	1,900	3.8	1.8	1.1	0.74
Settling time [ns]	100	3,000	9,000	1,600	1,240	62	65	45	53

N.R.= Not Reported

* For large current DLDOs, the edge rate is mainly limited by the input voltage droop due to parasitics during large load transient. The input voltage droop in lower-current DLDOs is typically less affected and can thus be tested at a higher edge rate.

† $\text{FoM} = \frac{C_{TOTAL} \cdot \Delta V_{OUT}}{\Delta I_L} \times \frac{I_Q}{\Delta I_L}$

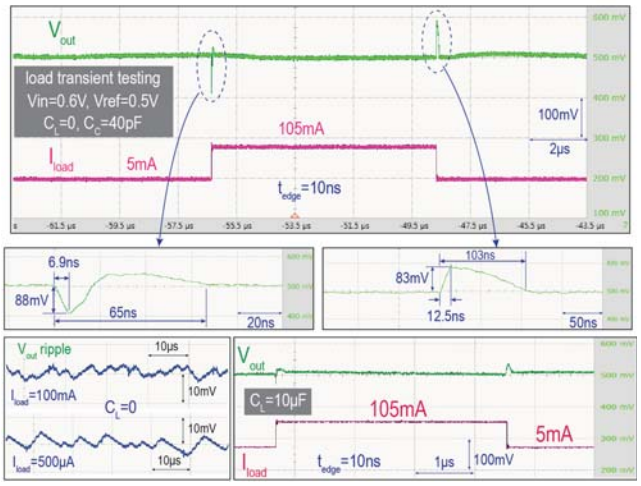


Fig. 7: Measured transient response of the proposed DLDO to a periodic load change with C_L=0 (top) and C_L=10μF (bottom-right); output voltage ripple with I_L=100mA and I_L=500μA (bottom-left).

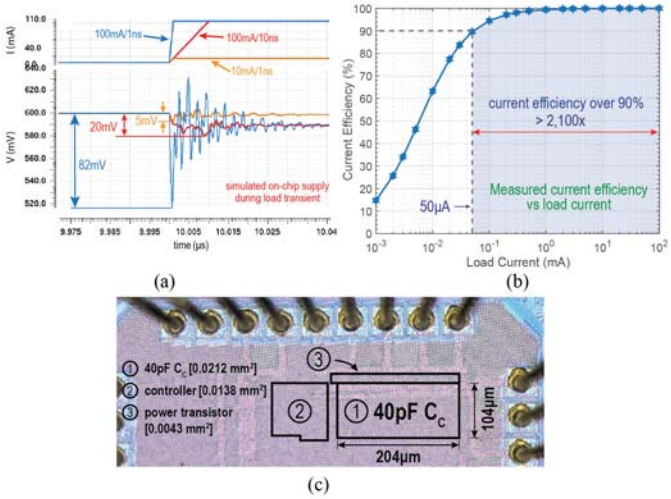


Fig. 8: (a) Simulated on-chip supply voltage droop during large load transient current (top-left), (b) measured current efficiency at 0.6V to 0.5V (top-right), (c). micrograph of the fabricated DLDO (bottom).

FoM. Despite this, at a 100mA/ns edge rate, the proposed DLDO still achieves a state-of-the-art FoM of 3.8fs, as shown in Table I. Thanks again to the ACHZ loop, the converter with C_L=10μF operates correctly without stability issues (Fig. 7, lower right). Thanks to the fine-tuning capabilities, sub-Vt detection, overflow current suppression, and g_m-adjusting weighted-CP-based design, ripple is measured to be <15mV at both I_{load}=100mA and 500μA in Fig. 7 (lower left), and a 105,000x stable load range (1μA to 105mA) is obtained. A current efficiency >90% is achieved over a 2,100x range from 50μA to 105mA (Fig. 8).

V. Conclusions

An event-driven charge pump based DLDO with ACHZ loop is presented in this paper. Thanks to the ACHZ loop and low-latency event-driven charge pump path, the DLDO can response less than a clock cycle and achieves a sub-4fs FoM. With the help of the overflow current suppression, sub-Vt detection and dynamic g_m-adjusting, the DLDO achieves a 105,000x stable load range (1μA to 105mA) and <15mV ripple.

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